Amendments to the Specification

Please replace the paragraph, beginning at page 1, line 5, with the following rewritten paragraph:

The present application is a divisional application of U.S. Application No. 09/187,730, filed on November 9, 1998, which claims the priority of ~~based on~~ U.S. Provisional Patent Application No. 60/065,082, filed November 10, 1997, the entire disclosure and contents of which is hereby incorporated by reference.

Please replace the paragraph, beginning at page 2, line 25, with the following rewritten paragraph:

According to one aspect of the present invention, there is provided a quantum ridge product comprising a substrate having a plurality of substantially parallel quantum ridges on a surface thereof, each pair of adjacent quantum ridges of the plurality quantum ridge having a pitch of 5.4 to 600Å and being separated by a groove having a width of ~~6~~ up to 597Å and a depth of 4 to 30,000Å, except ridge pitches from 5.4 to 9.3Å will support quantum wires but will not support stable grooves to be etched in Silicon (Si). All the ranges refer to Si and must be increased or decreased by up to 30% for other crystals.

Please replace the paragraph, beginning at page 3, line 4, with the following rewritten paragraph:

According to a second aspect of the present invention, there is provided a quantum ridge product comprising: a substrate having a plurality of substantially parallel quantum ridges on a surface thereof, each pair of adjacent quantum ridges of the plurality quantum ridge having a pitch of 5.4 to 600Å, and ridges with pitches of 9.4Å or larger being separated by a groove having a width of 6up to 597Å, at least one of the quantum ridges having a quantum wire supported on top of at least one of the quantum ridges and extending in a direction along the length of the quantum ridge, the quantum wire comprising a conductive material having a width of 3 to 594Å.

Please replace the paragraph, beginning at page 3, line 13, with the following rewritten paragraph:

According to a third aspect of the present invention, there is provided a quantum tip product comprising a substrate having a plurality of quantum tips on a surface thereof, each of the plurality of quantum tips being separated from an adjacent quantum tip by grooves, each of the grooves having a width of 6up to 597Å and a depth of 4 to 30,000Å.

Please replace the paragraph, beginning at page 3, line 19, with the following rewritten paragraph:

According to a fourth aspect of the present invention there is provided a quantum tip product comprising a substrate having a plurality of quantum tips on a surface thereof, each of the plurality of quantum tips being separated from adjacent quantum tips by grooves, each of the grooves having a width of up-6 to 597Å, at least one of the quantum tips having a quantum dot supported on top of at least one quantum tip, the quantum dot comprising a conductive material having a width of 3 to 594Å.

Please replace the paragraph, beginning at page 3, line 26, with the following rewritten paragraph:

According to a fifth aspect of the present invention, there is provided a method for making a quantum structure product comprising the steps of: providing a first substrate having a (1 1 X) surface structure and including a plurality of substantially parallel quantum ridges and grooves on a surface thereof, the grooves having a width of 6up to 597Å and separating adjacent quantum ridges; and coating the first substrate with a metal to form at least one quantum wire on at least one of the quantum ridges, the at least one quantum wire having a width of 3 to 47Å.

Please replace the paragraph, beginning at page 4, line 4, with the following rewritten paragraph:

According to a sixth aspect of the present invention, there is provided a quantum ridge product comprising two quantum ridge substrates bonded to each other, each of the substrates having a plurality of substantially parallel quantum ridges on a surface thereof, each pair of adjacent quantum ridges of the plurality quantum ridge having a pitch of 5.4 to 600Å and being separated by a groove having a width of ~~6~~up to 597Å and a depth of 4 to 30,000Å, the quantum ridge substrates being bonded together at the quantum ridge surface of each substrate.

Please replace the paragraph, beginning at page 4, line 12, with the following rewritten paragraph:

According to a seventh aspect of the present invention, there is provided a quantum ridge product comprising: a substrate having a plurality of substantially parallel quantum ridges on a surface thereof, each pair of adjacent quantum ridges of the plurality quantum ridges having a pitch of 5.4 to 600Å and being separated by a groove having a width of ~~6~~ up to 597Å, at least one of the quantum ridges having a quantum dot supported on top of the at least one quantum ridge, the quantum dot comprising a conductive material having a width in at least one direction of 3 to 594Å.

Please replace the paragraph, beginning at page 5, line 1, with the following rewritten paragraph:

According to a tenth aspect of the present invention, there is provided a quantum structure product comprising a substrate including a groove having a width of ~~6~~ up to 597Å and a depth of 4 to 30,000Å.

Please replace the paragraph, beginning at page 5, line 5, with the following rewritten paragraph:

There are three general ~~rages~~ ranges for the pitches of the present invention. For the Self Aligned Atomic Shadowing (SALAS) procedure, the range is preferably 5.4 to 54Å for quantum wires and quantum dots, and is 9.4 to 54Å for SALAS when ~~groves~~ grooves are etched or when quantum tips or dots are produced. The range of pitches for

the Self Aligned Atomic STEPS (~~SALASETPS~~SALASTEPS) is typically 54 to 600Å. It should be appreciated that there is some overlap between the ranges of SALAS and SALASTEPS. The SALASTEPS pitches and local separations are somewhat variable due to the ragged single layer and double layer atomic steps, but ~~he~~ the SALAS ridges are atomically straight and precisely spaced on the (1 1 4) surface of Si. The SALAS ridges on the (5 5 12) and other (1 1 X) surfaces may have restructuring faults, but the ridges are atomically straight over long distances.

Please replace the paragraph, beginning at page 6, line 17, with the following rewritten paragraph:

Figure 8 is a cross-sectional view of quantum wire material deposited on a portion of a terraced substrate having single layer atomic steps and obliquely evaporated deposition froom the right;

Please replace the paragraph, beginning at page 6, line 21, with the following rewritten paragraph:

Figure 9 is a cross-sectional view of a portion of a quantum-wire quantum-ridge product formed using a substrate having double layer atomic steps and obliquely evaporated deposition froom the right;

Please replace the paragraph, beginning at page 8, line 5, with the following rewritten paragraph:

For the purposes of the present invention, the term "channel" refers to the fact that all of the quantum ridges on a (1 1 X) surface in preferred substrates of the present invention, which comprise diamond and zincblende lattices, are in the "best" channeling direction of a single crystal in these diamond and zincblende lattices, namely ~~the (1 1 0) a~~ <1 1 0> direction for (1 1 X) surfaces. For the purposes of the present invention, the term "single channel wall thickness" or "SCWT" refers to the minimum thickness for the narrowest ridge for a particular substrate type, such as the quantum ridges 42 of Figure 4.

In silicon products, ridges that are thicker than the SCWT will have thicknesses of an integral multiple of 3.14Å when measured across their narrowest cross section.

Please replace the paragraph, beginning at page 17, line 19, with the following rewritten paragraph:

The second wafer may then be aligned perpendicular (or at some other specified angle) to the first wafer, substrate, and pressed carefully onto the surface of the first wafer. The wafers are allowed to contact each other without any significant lateral shifting by first contacting the flat bottom edges of the otherwise circular wafers and then letting gravity close them like closing a book. The Van der Waals forces between the two surfaces then finishes the bonding process so that there is no lateral shifting of the wafers. To ensure that the quantum wires are completely cut, a weight may be placed on the wafer sandwich. This bonding process may be accomplished by any of the standard methods, for example, in air, in an inert gas, in a vacuum, or in a liquid such as deionized water, dilute HF, alcohol, or other chemical. The preferred ambient solution for producing quantum dots is dilute HF.

Please replace the paragraph, beginning at page 19, line 29, with the following rewritten paragraph:

In addition to forming quantum dots on quantum tips, the present invention provides quantum dots formed on quantum ~~tips~~ridges. Such quantum dot-quantum ridge products may be formed by using deep groove quantum wire product of the present invention and cutting the quantum wires using a second wafer having quantum ridges thereon as described above for forming quantum dots on quantum tips. Figure 6 shows a quantum dot-quantum ridge product 60 of the present invention in which quantum dots 62 are supported on quantum ridges 64. Quantum ridges 64 are separated by a groove 66. For simplicity, only two of the ridges and only a portion of substrate 68 of the quantum dot-quantum ridge product is shown in Figure 6. A quantum dot-quantum ridge product of the type shown in Figure 6 may also be used as a precursor for forming a deep groove quantum dot-quantum tip product or a deep groove quantum tip product by etching

substrate material from the portions of the quantum ridges which are not protected by the quantum dots.

Please replace the paragraph, beginning at page 20, line 22, with the following rewritten paragraph:

A preferred method to produce depressions is to use $KOH:H_2O$ to thin a wafer by a small amount (2.5 μm) after introducing small etch pit (0.5 μm in diameter). After thinning this small amount, the etched depression is extremely smooth and has a diameter of 10 μm with a sagitta of only 0.18 μm. The surface quality near the bottom of the depression is nearly atomically flat after this very simple process. This atomically flat region may then by enlarged by a touch up with normal chem-mechanical polishing CMP step, and/or by heating the sample in UHV for 75 minutes at 1150°C. Large atomically flat regions may also be formed in UHV by Ar ion bombardment at 950°C for less than 5 minutes. A much exaggerated view and two different convex regions are shown in Figure 7 after a brief (5 minute) CMP process. This is preferably followed by an Ar ion bombardment in UHV for 3 to 5 minutes to expand the atomically flat regions to several μm width and length, which is more than large enough to place the gate regions of nMOS or pMOS transistors. The atomically flat regions are emphasized by dark lines in Figure 7. Figure 7 shows a cross-sectional view of a substrate 72 having depressions 74 with flat regions 75 and convex regions 76 with flat regions 77. The depressions and convex regions may be oblong along the quantum ridge directions, or perpendicular to the quantum ridges, or at arbitrary angles to the ridges for particular applications. For example, the source and drain regions may be quite wide relative to the length, which is desirable for a high transconductance.

Please replace the paragraph, beginning at page 22, line 21, with the following rewritten paragraph:

The quantum ridges of the present invention preferably have a width of about 3 to 594Å. The center line-to-center line separations or "pitch" for each pair of adjacent quantum ridges is preferably 5.4 to 600Å, most preferably 9.4 to 54Å. The grooves of the

present invention preferably have a depth of 4 to 30,000Å. The 4Å lower limit for the preferred groove depth is chosen by assuming that a single row of atoms is removed from the grooves of the restructured surfaces of a Si substrate all along their length. If no atoms are removed from the restructured surfaces, the deepest depressions in the restructured surfaces are generally about 3Å for Si (5 5 12) and about 2Å for Si (1 1 4). This small amount (4Å) of surface undulation will be useful in some applications. A pitch of 6.4Å for Si (113) and 5.4Å for Si (110) are possible and are useful for quantum wire spacings. However, if atoms are removed from the two-channel-wall thicknesses of 6.4Å. ~~To~~ to attempt to produce grooves, the walls may be subject to collapse. Thus, a preferred pitch between quantum ridges is 9.4Å when the grooves in a substrate are to be deepened, thereby allowing a double channel width groove to be etched (or ion bombarded) having a width as small as 6.3Å, which is generally rounded to 6Å. The grooves of the present invention are preferably 6Å to 51Å in width. For quantum structure products of the invention in which the grooves between ridges or tips are etched, the grooves preferably have a depth of 4 to 30,000Å. For grooves having a width of 6 to 51Å, a preferred depth is 4 to 3000Å in order to maintain stability of the grooves and ridges.

Please replace the paragraph, beginning at page 25, line 15, with the following rewritten paragraph:

In some embodiments of the present invention it is desirable to at least partially fill the grooves of the quantum ridge or tip product of the invention with buckyballs, either C_{36} or C_{60} (fullerene balls) or buckytubes (fullerene tubes), as shown in Figure 5. Methods for producing fullerene balls and tubes suitable for use in the present invention are well known. Quantum structure products of the present invention including fullerene balls tightly packed into the grooves which may be use for producing superconductors. For example, three alkali metal atoms may be packed into a groove for every Fullerene molecule to form a silicon intercalated superconductor. When the substrate of the present invention is made from silicon, the quantum ridges and tips of the present invention may be doped with phosphorus and boron. to modify the critical temperature and other superconducting properties.

Please replace the paragraph, beginning at page 26, line 18, with the following rewritten paragraph:

An appropriately oriented sample of Si, a (5 5 12) wafer, is prepared by standard chem-mechanical polishing methods. The wafer is placed in a UHV chamber which is pumped to a vacuum of about 10^{-10} torr. The Si is then heated to 1150° C for a brief period ("flashed") to remove any surface oxides and then cooled to below room temperature (around -20° to 25° C~~900° C~~). The heating of the wafer may also be accomplished locally using a focused or beam-expanded laser passing through a quartz window in the MBE machine. This leaves the surface in a stable condition with slightly elevated ridges separated in Å by 16, 22, 16; 16, 22, 16, with this sequence of 54Å width persisting over significant distances in regions where the heating occurs, and with the ridges also reaching across the whole length of the wafer. The ridges have occasional steps in them along their length due to the slight variations from perfect flatness of the wafer surface, but after each step, the ridges again establish themselves in the same <1 1 0> direction. In addition, there are occasional surface faults in the (5 5 12) sequence that disrupt the regularity of the 16,22,16, or 54Å unit cell, repetitions. These faults have a missing 16Å section, with the fault then effectively having only a 38Å section instead of a 54Å sequence. By contrast, the other good ridge forming plane, the (1 1 4), has very regular 16.3Å spacing with no surface faults.

Please replace the paragraph, beginning at page 27, lines 6, with the following rewritten paragraph:

Some low melting point metals must be deposited on the crystalline substrates at much lower temperatures (at least as low as 64°K for some metals~~RB~~) to ensure that surface diffusion does not cause the metal to agglomerate and compromise the atomic ridge deposition of the SALAS process. Still, other metals have measurable surface diffusion on semiconductor and other crystal surfaces near room temperature and are not good candidates for SALAS process except at very low substrate temperatures. However, a modest heat treatment after room temperature deposition in the UHV/MBE system may sometimes result in well formed ridges on one or more sets of the different ridge-type

bonding sites on (1 1 X) surfaces. For example, Au ~~bill~~ will diffuse to such sites at a temperature as low as 250°C, even though the eutectic temperature is 363°C. Subsequent heating to 700°C or higher may result in Vapor Liquid Solid (VLS) growth of quantum studs and wires shown in Figures 2 and 9. This may be done using gas assisted epitaxy using Si_2H_6 in the MBE machine.